

requirement for lower cost and power consumption. The challenge for the semiconductor industry is to develop a disruptive packaging technology capable of achieving these goals.

To meet the above said challenges, eWLB is a continually evolving technology platform which offers additional space for routing higher I/O chips on top of the silicon (Si) chip area which is not possible in conventional wafer level packaging (WLP) or wafer level backa4[ptiob(o)5(og)] TJETBT0:050299999 Tc013438 TwI4145 TLIO.001 0 0 10.02 48.243

2) The singulated die are accurately placed face down

Table 3 shows the package level reliability result of 3D eWLB-PoP. They passed JEDEC (Joint Electron Device Engineering Council) standard package reliability tests such as MSL (Moisture Sensitivity Level) 3 with Pb-free solder conditions. The test vehicles (TV1/2) were 10x10mm and 15x15mm 3D eWLB-PoP. Both successfully passed all industry standard package level reliability with ball shear test and OS test.

Table 3. Package Level Reliability Results of 3D eWLB-PoP.

Reliability Test	JEDEC	Test Condition	Read-out	Results
MSL	JESD22-A103	-55/125°C, 2000hr	1000hr	Temperature Cycle (TCT), w/MSL
High Temp. Stc	JESD22-A103	150°C	1000hr	High Temp. Stc (HTS)
Pass				

Experimental Thermal Characterization of 3D eWLB-PoP

For thermal characterization, the test vehicle was prepared with thermal die. Test vehicle specification was same as TV2 in Table 2(b). In this study, die thickness effect was studied with 3 different die thicknesses: 200um, 300um and 400um. The same die sizes for fcPoP were prepared for the comparison study.

All test vehicles had thermal die with a transistor and heating circuit block as well as temperature sensor so it easily detected temperature at the hot spot of the die with applied power. After SMT on thermal test PCB, 2.0W power was applied and measured junction temperature with various die thickness. As shown in Figure 5, eWLB-PoP has 8-10% thermal performance improvement for the same die thickness as compared to fcPoP. For eWLB, it can use thicker die than fcPoP for embedding, achieving a >20% improvement in thermal performance with the same package height of eWLB-PoP compared to fcPoP.

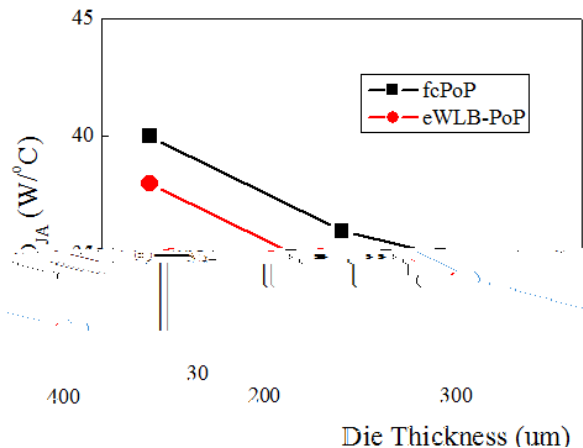


Figure 5. Thermal characterization data of 3D eWLB-PoP with different die thickness compared to fcPoP.

Electrical Functional Characterization of 3D eWLB-PoP

The TV1 and TV2 were assembled with Live dice from 28nm Low Power Foundry technology. After assembling the 3D eWLB PoP, final functional test, bench test and system level test (SLT) were performed with existing test infrastructure including test hardware of fcPoP. Test was also carried out at room temperature and hot-test of 110°C. Both TV1, TV2 passed SLT testing and all Stress tests (MSL3,TC, HTS) as shown in Table 3.

Test data shows 3D eWLB-PoP performance is equivalent or slightly improved compared to fcPoP solutions. Multiple retests did not result in cracking and it proved the mechanical robustness of low profile 3D eWLB-PoP.

Parasitic Electrical Simulation of 3D eWLB-PoP and fcPoP

The RLC parasitic values for eWLB-PoP and fcPoP were extracted by computer simulation using commercial 2D electromagnetic field solver. The S-parameter of each packages were extracted by using ANSOFT HFSS. Simulated results are compared with RLC parasitic values and S parameters. The simulation modeling design was carried out with functional devices to investigate package level performance in real applications. In 3D simulation works, a few critical pins were selected and studied, such as clock, VDD as well Data pins.

Table 4. Electrical parasitic values of RL of eWLB-PoP and fcPoP @ 1GHz. :

Inductance, L (nH)		Resistance, R (mΩ)	
1	0.57	1.0	1.51
2	0.25	0.66	1.08
3	0.25	0.66	1.08
4	0.25	0.66	1.08
5	0.25	0.66	1.08
6	0.25	0.66	1.08
7	0.25	0.66	1.08
8	0.25	0.66	1.08
9	0.25	0.66	1.08
10	0.25	0.66	1.08

Board Level Reliability of 3D eWLB-PoP

For board level reliability tests, eWLB-PoP (stacked with top package) was assembled and mounted on the PCB. For PoP assembly, 0.4mm body thickness FBGA top packages were assembled and the total eWLB-PoP stacked package was less than 0.8mm in height after SMT on PCB. Those samples were tested in JEDEC TCob and drop reliability test conditions.

Table 4 shows 3D eWLB-PoP board level reliability of JEDEC TCob and drop test results of test vehicle 1 and 2 (Table 2 and Figure 3). The first TCob failure was after 1000 cycles. Drop reliability performance was robust and showed no failure after 300 drops. These test results show the robustness of board level reliability of 3D eWLB-PoP.

Figure 6. Micrographs of cross-section of 3D eWLB-PoP stacked after top package attachment.

Table 4. Board Level Reliability Test Results of 3D eWLB-PoP

Tests	Conditions	Status
TCoB	JEDEC JESD22-A103 -40°C to 125°C	Pass
Drop Test	JEDEC JESD22-B111 1500G	Pass

3D eWLB SiP / Module

FO-WLP in a 3D configuration has received considerable customer interest for memory and advanced application processors by virtue of the higher routing density and form factor reduction. The requirement for SiP integration is also a growing trend for advanced application processors, MEMS and sensors in IoT/WE as way to cost-effectively achieve advanced silicon die partitioning for increased performance and integration in a reduced form factor[5].

(a)

(b)

Figure 7. Schematics of 3D eWLB SiP: (a) with interposer and (b) discretes on interposer or top package of discretes.

Figure 8. Micrographs of 3D eWLB SiP with interposer

Figure 7 shows one of example of 3D eWLB SiP/module which that has a number of discretes in the top package and is pre-stacked on the bottom eWLB to form a 3D SiP/module with a thin profile. Discretes were removed from the motherboard and relocated in the top package for a reduction in the space required on the mother board. Discretes are also more effective when they are close to the device, which significantly improves the overall performance as well as

semiconductor packages with increased performance and packaging complexity. Wafer level technology effectively accommodates new lithography foundry technology nodes and provides a strong packaging platform to address performance, form factor, integration and cost requirements. In addition to providing higher bandwidth, ultra high density, embedded capabilities, and improved thermal dissipation in a small, thin package format, advanced wafer level packaging is an alternative for small flip-chip and large QFN packages and is quickly becoming a package of choice in the evolving mobile, IoT and WE markets. Fan-out wafer level technology also provides the ability to tightly manage the co-design process and achieve silicon optimization, which is increasingly important in ultra cost-sensitive markets.

Advanced packaging plays a crucial role in delivering achieving higher performance, lower power, lower cost, and a smaller form factor. There are many challenges that have been, and are being resolved in the application of cost-effective materials and processes for various reliability and security requirements for new and emerging mobile, IoT and WE applications. The industry requires innovation in packaging technology and a cost-effective, high-volume manufacturing process that is able to meet current and forecasted market demands.

eWLB technology is an important wafer level packaging solution that will enable the next generation of mobile applications. The advantages of standard fan-in WLPs, such as low assembly cost, minimum dimensions and height, as well as excellent electrical and thermal performance, are equally true for eWLB. The differentiating factors with eWLB are the ability to integrate passives like inductors, resistors and capacitors into the various thin-film layers, active/passive devices into the mold compound, and achieve 3D vertical interconnections for new SiP and 2.5D/3D packaging solutions. Advanced eWLB technology will play an important role in the new wave of IoT and WE devices today, and in the near future.

Advanced low profile 3D eWLB-PoP was developed using eWLB (FO-WLP) technology. It passed JEDEC standard component level reliability conditions. PoP package stacking and board level reliability were carried out and showed robust reliability in TCoB and drop tests. Thermal and functional electrical characterizations were carried out and showed the enhanced performance of 3D eWLB-PoP compared to fcPoP.

3D eWLB-PoP / eWLB SiP technology provides more performance value add and is proving to be a new packaging platform that can expand its application range to various types of emerging mobile, IoT and WE devices as well as 3D SiP systems.

References

[1] M. Brunnbauer, et al., "Emberdded Wafer Level Ball Grid Array (eWLB)," Proceedings of 8th Electronic Packaging Technology Conference, 10-12